MODULE DESCRIPTION FORM

نموذج وصف المادة الدراسية

Module Information معلومات المادة الدراسية					
Module Title	**Digital Electronics / الإلكترونيك الرقمي**			**Module Delivery**	
Module Type	**Core**			☒ **Theory** ☒ **Lecture** ☒ **Lab** ☐ **Tutorial** ☐ **Practical** ☐ **Seminar**	
Module Code	**CYBT106**				
ECTS Credits	**8**				
SWL (hr/sem)	**200**				
Module Level			**Semester of Delivery**	2	
Administering Department	Cybersecurity Technical Engineering / قسم الأمن تقنيات هندسة السيبراني		**College**	Technical Engineering College of Computer and AI - Kirkuk / التقنية الكلية كركوك - الاصطناعي والذكاء للحاسوب الهندسية	
Module Leader	Dr. Academic Leader		**e-mail**	leader@ntu.edu.iq	
Module Leader's Acad. Title	Assistant Professor		**Module Leader's Qualification**		Ph.D. in Electronics / Electrical Engineering
Module Tutor	Tutor Name		**e-mail**	tutor@ntu.edu.iq	
Peer Reviewer Name	Reviewer Name		**e-mail**	reviewer@ntu.edu.iq	
Scientific Committee Approval Date	01/09/2024		**Version Number**	1.0	

Relation with other Modules العلاقة مع المواد الدراسية الأخرى

Prerequisite module	Fundamentals of Electrical Engineering / Physics (CAIK100)	**Semester**	1 & 2
Co-requisites module	Computer Architecture and Organization / Embedded Systems	**Semester**	3 & 4

Module Aims, Learning Outcomes and Indicative Contents أهداف المادة الدراسية ونتائج التعلم والمحتويات الإرشادية	
Module Aims أهداف المادة الدراسية	This module aims to provide engineering students with fundamental concepts and practical skills in digital electronics and logic design. It covers number systems and codes, Boolean algebra, logic gates, combinational logic circuits (adders, multiplexers, decoders), sequential logic design (flip-flops, counters, shift registers), semiconductor memories, digital-to-analog and analog-to-digital converters, and practical circuit implementation using logic ICs and simulation software.
Module Learning Outcomes مخرجات التعلم للمادة الدراسية	Understand number systems (Binary, Octal, Hexadecimal) and binary codes (BCD, Gray, ASCII). Apply Boolean algebra, De Morgan's theorems, and Karnaugh maps (K-maps) to simplify logic functions. Design and analyze combinational logic circuits including adders, subtractors, encoders, decoders, multiplexers, and demultiplexers. Analyze sequential logic circuits, flip-flops (SR, JK, D, T), latches, counters, and shift registers. Comprehend digital circuit families (TTL, CMOS) and semiconductor memory devices (ROM, RAM). Understand basic principles of DAC and ADC conversions in electronic communication systems. Construct, test, and troubleshoot digital logic circuits in hardware laboratory sessions using breadboards and ICs.
Indicative Contents المحتويات الإرشادية	The module will cover the following key areas: Number Systems & Codes: Binary, Octal, Hexadecimal Systems, Conversions, 1's and 2's Complements, Binary Arithmetic Boolean Algebra & Logic Gates: Basic Gates (AND, OR, NOT), Universal Gates (NAND, NOR), XOR/XNOR, and Truth Tables Simplification of Logic Functions: Algebraic Simplification, Sum of Products (SOP), Product of Sums (POS), and Karnaugh Maps (2, 3, 4 variables) Combinational Logic Circuits I: Half Adders, Full Adders, Half/Full Subtractors, Parallel Adders, and Look-Ahead Carry Adders Combinational Logic Circuits II: Encoders, Decoders, Multiplexers (MUX), Demultiplexers (DEMUX), and Magnitude Comparators Sequential Logic Circuits I: Latches, Flip-Flops (SR, JK, D, T Flip-Flops), Triggering Methods, and Master-Slave Flip-Flops Sequential Logic Circuits II: Registers, Shift Registers (SISO, SIPO, PISO, PIPO), and Universal Shift Registers

	Counters & Sequential Analysis: Asynchronous (Ripple) Counters, Synchronous Counters, Up/Down Counters, and Modulo Counters Logic Integrated Circuit Families: TTL, CMOS Characteristics, Propagation Delay, Fan-Out, and Power Dissipation Semiconductor Memories & Data Converters: ROM, RAM, PAL/PLA Basics, DAC and ADC Architecture Principles

Learning and Teaching Strategies استراتيجيات التعلم والتعليم	
Strategies	The module will employ a combination of strategies including: Lectures: To present theoretical concepts of number systems, Boolean algebra, logic simplification, and circuit design. Problem-Solving Sessions: Step-by-step guidance on Karnaugh map minimization, truth table construction, and timing diagrams. Practical Laboratory Sessions: Hands-on breadboard wiring of digital ICs, testing logic gates, and hardware verification. Software Simulation Exercises: Simulating digital circuits using tools like Proteus or Multisim prior to physical testing. Mid-term and final exams: To evaluate theoretical understanding and practical digital logic implementation skills. Preparatory Week: To give students time to revise and clarify any design difficulties before the final exam.

Student Workload (SWL) الحمل الدراسي للطالب محسوب لـ ١٥ اسبوعا			
Structured SWL (h/sem) الحمل الدراسي المنتظم للطالب خلال الفصل	63	**Structured SWL (h/w)** الحمل الدراسي المنتظم للطالب أسبوعيا	4
Unstructured SWL (h/sem) الحمل الدراسي غير المنتظم للطالب خلال الفصل	62	**Unstructured SWL (h/w)** الحمل الدراسي غير المنتظم للطالب أسبوعيا	4
Total SWL (h/sem) الحمل الدراسي الكلي للطالب خلال الفصل	125		

Module Evaluation تقييم المادة الدراسية				
	Time/Number	**Weight (Marks)**	**Week Due**	**Relevant Learning Outcome**

Formative assessment	**Quizzes**	2	5% (5)	5, 10	LO #1, 3 and 5
	Assignments	2	5% (5)	2, 12	LO #2, 4 and 6
	Projects / Lab.	1	10% (10)	Continuous	LO #7
	Report	1	10% (10)	13	LO #3, 5 and 7
Summative assessment	**Midterm Exam**	2 hr	20% (20)	8	LO #1 - 4
	Final Exam	2hr	50% (50)	16	All
Total assessment			100% (100 Marks)		

Delivery Plan (Weekly Syllabus)

المنهاج الاسبوعي النظري

	Material Covered
Week 1	Introduction to Digital Electronics: Analog vs. Digital Signals, Binary Logic Levels, and Digital Applications.
Week 2	Number Systems & Conversions: Binary, Octal, Hexadecimal, BCD, Gray Code, and Binary Arithmetic.
Week 3	Logic Gates & Truth Tables: AND, OR, NOT, NAND, NOR, XOR, XNOR Gates, and Universal Logic Concept.
Week 4	Boolean Algebra Principles: Boolean Laws, Theorems, De Morgan's Theorems, and Duality Principle.
Week 5	Simplification of Boolean Functions I: Canonical Forms (SOP and POS) and Algebraic Simplification Techniques.
Week 6	Simplification of Boolean Functions II: Karnaugh Maps (K-maps) for 2, 3, and 4 Variables, Don't Care Conditions.
Week 7	Combinational Logic Circuits I: Design Procedure, Half Adder, Full Adder, Half Subtractor, and Full Subtractor.
Week 8	Mid-term Exam (الفصل منتصف اختبار) & Parallel Binary Adders, Carry Look-Ahead Adders, and BCD Adders.
Week 9	Combinational Logic Circuits II: Decoders, Encoders, Priority Encoders, Seven-Segment Display Decoders.
Week 10	Combinational Logic Circuits III: Multiplexers (MUX), Demultiplexers (DEMUX), and Logic Design using MUXs.
Week 11	Sequential Logic Circuits I: Difference between Combinational and Sequential Circuits, SR Latches, and Clocked Latches.
Week 12	Sequential Logic Circuits II: SR, JK, D, and T Flip-Flops, Master-Slave Configuration, and Characteristic Equations.

Week 13	Registers & Shift Registers: SISO, SIPO, PISO, PIPO Shift Registers, Ring Counters, and Johnson Counters.
Week 14	Asynchronous Counters: Design and Analysis of Ripple Counters, Modulo-N Counters, and Up/Down Counters.
Week 15	Synchronous Counters & Logic IC Families: Synchronous Counter Design, TTL/CMOS Electrical Characteristics.
Week 16	Semiconductor Memories, DAC/ADC Fundamentals, Course Review & Final Examination (الاختبار النهائي).

Delivery Plan (Weekly Lab. Syllabus) المنهاج الاسبوعي للمختبر	
	Material Covered
Week 1	Lab 1: Introduction to Digital Logic Trainer Boards, Breadboards, Logic ICs (7400 Series), and Logic Probe Usage.
Week 2	Lab 2: Verifying Truth Tables of Basic Logic Gates (AND, OR, NOT, NAND, NOR, XOR, XNOR ICs).
Week 3	Lab 3: Implementing Universal Logic Gates (NAND/NOR Logic Realization) and De Morgan's Laws Verification.
Week 4	Lab 4: Design and Implementation of Half Adder and Full Adder Circuits using Basic Gates and ICs.
Week 5	Lab 5: Design and Testing of Multiplexer (74151/74153) and Decoder (74138) Circuits.
Week 6	Lab 6: Testing Flip-Flop ICs (7474 D Flip-Flop, 7476 JK Flip-Flop) and Asynchronous Counter Assembly (7490).
Week 7	Lab 7: Revision, Practical Circuit Troubleshooting, Practical Hardware Exam, and Course Assessment.

Learning and Teaching Resources مصادر التعلم والتدريس		
	Text	**Available in the Library?**
Required Texts	Mano, M. M., & Ciletti, M. D. (2018). "Digital Design: With an Introduction to the Verilog HDL, VHDL, and SystemVerilog" (6th ed.). Pearson.	Yes
Recommended Texts	Floyd, T. L. (2015). "Digital Fundamentals" (11th ed.). Pearson.	Yes
Websites	Yes	

Grading Scheme مخطط الدرجات				
Group	**Grade**	التقدير	**Marks (%)**	**Definition**
Success Group (50 - 100)	**A** - Excellent	امتياز	90 - 100	Outstanding Performance
	B - Very Good	جيد جدا	80 - 89	Above average with some errors
	C - Good	جيد	70 - 79	Sound work with notable errors
	D - Satisfactory	متوسط	60 - 69	Fair but with major shortcomings
	E - Sufficient	مقبول	50 - 59	Work meets minimum criteria
Fail Group (0 – 49)	**FX** – Fail	راسب (قيد المعالجة)	(45-49)	More work required but credit awarded
	F – Fail	راسب	(0-44)	Considerable amount of work required

Note: Marks Decimal places above or below 0.5 will be rounded to the higher or lower full mark (for example a mark of 54.5 will be rounded to 55, whereas a mark of 54.4 will be rounded to 54. The University has a policy NOT to condone "near-pass fails" so the only adjustment to marks awarded by the original marker(s) will be the automatic rounding outlined above.